# **74AHCT17A**

# Hex buffer Schmitt trigger

Rev. 2 — 7 August 2023

**Product data sheet** 

### 1. General description

The 74AHCT17A is a hex buffer with Schmitt-trigger inputs, capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

Designed to operate over a  $V_{CC}$  range from 4.5 V to 5.5 V, the inputs are TTL compatible. This range allows the device to be used to translate from 3.3 V to 5 V.

This device is fully specified for partial Power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

### 2. Features and benefits

- · Direct interface with TTL levels
- Supply voltage range from 4.5 V to 5.5 V
- Typical t<sub>pd</sub> of 3.2 ns at 5 V
- Typical  $V_{OL(p)}$  < 0.8 V at  $V_{CC}$  = 5 V,  $T_{amb}$  = 25 °C
- Typical  $V_{OH(v)} > 2.3 \text{ V}$  at  $V_{CC} = 5 \text{ V}$ ,  $T_{amb} = 25 ^{\circ}\text{C}$
- · Supports mixed-mode voltage operation on all ports
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 3000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

# 3. Ordering information

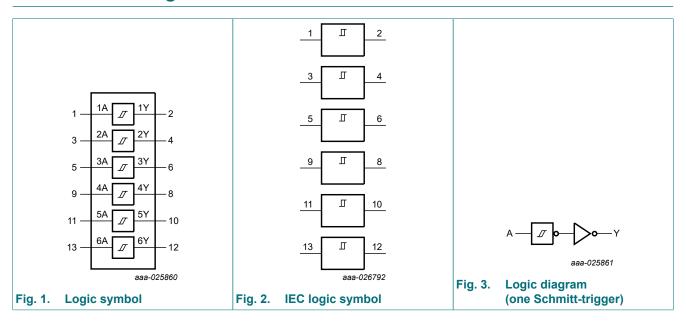
### **Table 1. Ordering information**

Type number	Package	ackage									
	Temperature range	Name	Description	Version							
74AHCT17APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1							



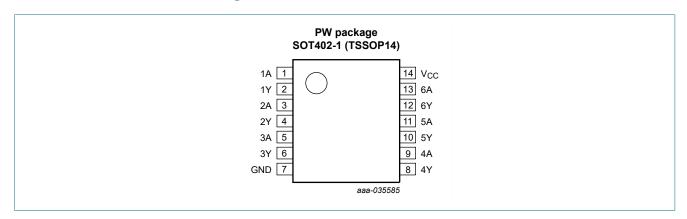
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# 4. Functional diagram



# 5. Pinning information

# 5.1. Pinning



# 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

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# 6. Functional description

#### Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$ 

Input	Output
nA	nY
L	L
Н	Н

# 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
VI	input voltage	[1	-0.5	+7.0	V
Vo	output voltage	output HIGH or LOW state [2][3	-0.5	V <sub>CC</sub> + 0.5	V
		output power-down [2	-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-20	-	mA
Io	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±25	mA
I <sub>CC</sub>	supply current		-	75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$	-	500	mW

<sup>[1]</sup> If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

# 8. Recommended operating conditions

### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		4.5	5.0	5.5	V
$V_{I}$	input voltage		0	-	5.5	V
Vo	output voltage	output HIGH or LOW state	0	-	V <sub>CC</sub>	V
		output power-down	0	-	5.5	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	1	ms/V

<sup>2]</sup> If the output current ratings are observed, the output voltage ratings may be exceeded.

<sup>[3]</sup> This value is limited to 7 V maximum.

<sup>[4]</sup> For SOT402-1 (TSSOP14) package: P<sub>tot</sub> derates linearly with 7.3 mW/K above 81 °C.

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# 9. Static characteristics

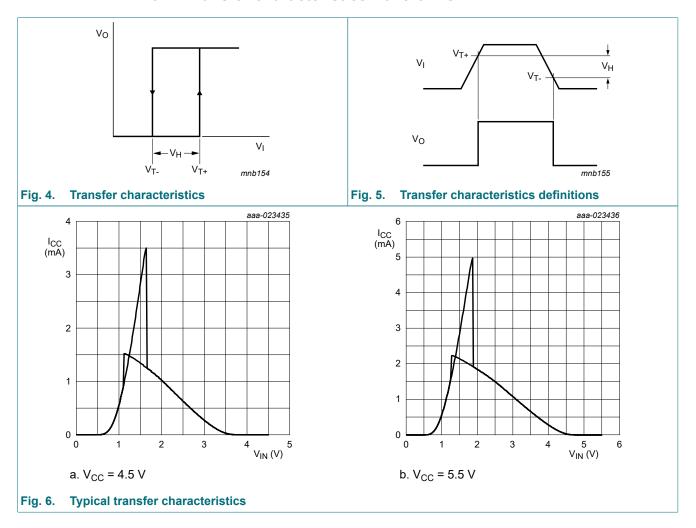
### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C	;	-40 °C to	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
V <sub>T+</sub>	positive-going	V <sub>CC</sub> = 4.5 V	-	-	1.9	-	1.9	-	1.9	V
	threshold voltage	V <sub>CC</sub> = 5.5 V	-	-	2.1	-	2.1	-	2.1	V
V <sub>T-</sub>	negative-going	V <sub>CC</sub> = 4.5 V	0.5	-	-	0.5	-	0.5	-	V
	threshold voltage	V <sub>CC</sub> = 5.5 V	0.6	-	-	0.6	-	0.6	-	V
V <sub>H</sub>	hysteresis	V <sub>CC</sub> = 4.5 V	0.4	-	1.4	0.4	1.4	0.4	1.4	V
voltage	V <sub>CC</sub> = 5.5 V	0.4	-	1.5	0.4	1.5	0.4	1.5	V	
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = -50 μA	4.4	-	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8 mA	3.94	-	-	3.8	-	3.7	-	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = 50 μA	-	-	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>OFF</sub>	power-off leakage current	$V_1$ or $V_0$ = GND to 5.5 V; $V_{CC}$ = 0 V		-	0.5	-	5	-	5	μA
I <sub>I</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 0$ V to 5.5 V		-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2	-	20	-	20	μΑ
Δl <sub>CC</sub>	additional supply current	per input pin; $V_{CC}$ = 5.5 V; $V_{I}$ = 3.4 V; $I_{O}$ = 0 A; other pins at $V_{CC}$ or GND	-	-	1.35	-	1.5	-	1.5	mA

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# 9.1. Transfer characteristics waveforms



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# 10. Dynamic characteristics

### **Table 7. Dynamic characteristics**

GND = 0 V. For test circuit, see Fig. 8.

Symbol	Parameter	Conditions	25 °C			-40 °C t	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t <sub>pd</sub>	propagation	nA to nY; see Fig. 7 [2]								
	delay	V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.2	8.3	1	9.9	1	10.6	ns
		C <sub>L</sub> = 50 pF	-	5.0	9.8	1	11.3	1	12.1	ns
C <sub>I</sub>	input capacitance	$V_I = V_{CC}$ or GND; $V_{CC} = 5 V$	-	2	6	-	6	-	6	pF
Co	output capacitance	$V_O = V_{CC}$ or GND; $V_{CC} = 5 \text{ V}$	-	5	-	-	-	-	-	pF
C <sub>PD</sub>	power dissipation capacitance	per buffer; $C_L = 0$ pF; [3] f = 10 MHz; $V_I = GND$ to $V_{CC}$	-	9.8	-	-	-	-	-	pF

<sup>[1]</sup> Typical values are measured at  $T_{amb}$  = 25 °C and  $V_{CC}$  = 5 V.

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in Volts.

#### **Table 8. Noise characteristics**

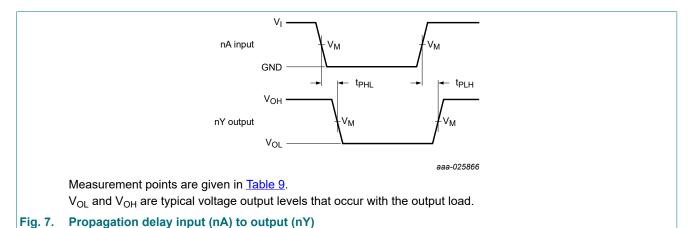
GND = 0 V. For test circuit, see Fig. 8.

Symbol	Parameter	Conditions	-	T <sub>amb</sub> = 25 °C			
			Min	Тур	Max		
V <sub>CC</sub> = 5	V; C <sub>L</sub> = 50 pF						
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.4	8.0	V	
$V_{OL(v)}$	LOW-level output voltage (valley)		-0.8	-0.2	-	V	
$V_{OH(v)}$	HIGH-level output voltage (valley)		-	4.5	-	V	
V <sub>IH(AC)</sub>	AC HIGH-level input voltage		2	-	-	V	
$V_{IL(AC)}$	AC LOW-level input voltage		-	-	0.8	V	

Typical values are measured at T<sub>amb</sub> = 23° C and V<sub>CC</sub> = 3 V.
 t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
 C<sub>PD</sub> is used to determine the dynamic power dissipation P<sub>D</sub> (μW).
 P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> + Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:

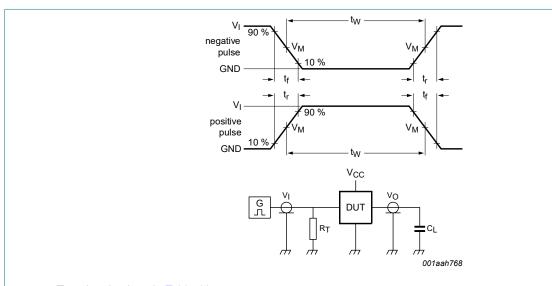
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### 10.1. Waveforms and test circuit



**Table 9. Measurement points** 

Input	Output
$V_{M}$	$V_{M}$
1.5 V	0.5V <sub>CC</sub>



Test data is given in Table 10.

Definitions test circuit:

 $R_{T}$  = Termination resistance should be equal to output impedance  $Z_{o}$  of the pulse generator;

 $C_L$  = Load capacitance including jig and probe capacitance.

Fig. 8. Test circuit for measuring switching times

Table 10. Test data

Input		Load	Test	
V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	CL		
GND to 3 V	3.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>	

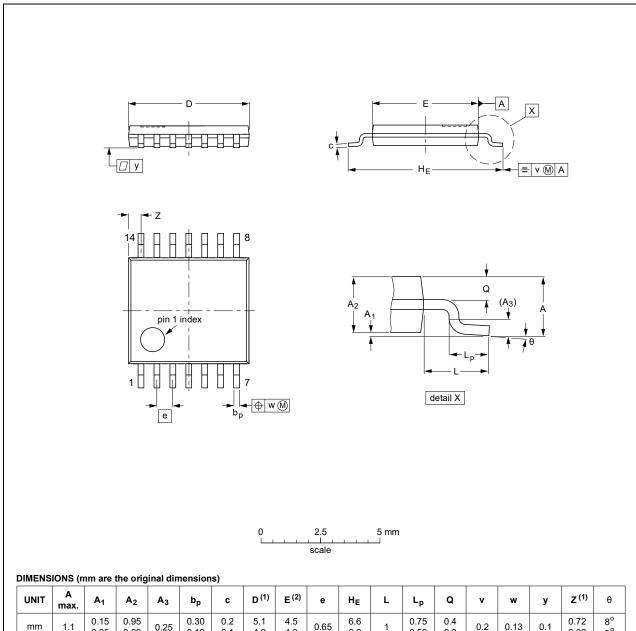
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# 11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	Α3	b <sub>p</sub>	С	D <sup>(1)</sup>	E <sup>(2)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				<del>99-12-27</del> 03-02-18

Fig. 9. Package outline SOT402-1 (TSSOP14)

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# 12. Abbreviations

### **Table 11. Abbreviations**

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
TTL	Transistor-Transistor Logic

# 13. Revision history

### **Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74AHCT17A v.2	20230807	Product data sheet	-	74AHCT17A v.1	
Modifications:	<ul> <li>Section 2: ESD specification updated according to the latest JEDEC standard.</li> <li>Section 7: Derating values for P<sub>tot</sub> total power dissipation updated.</li> </ul>				
74AHCT17A v.1	20170518	Product data sheet	-	-	

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### 14. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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